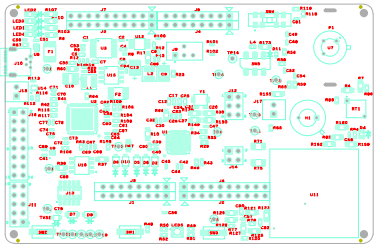
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
01	PROTO RELEASE	01/06/15	AKAP
02	ALPHA RELEASE	01/27/16	AKAP
03	BETA RELEASE	02/03/16	AKAP
04	ES10 RELEASE	02/09/16	AKAP
05	ES10 RELEASE	02/20/16	AKAP
06	ES10 RELEASE	02/26/16	AKAP



UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ON: ANGLES +/- 2°
2 PL DECIMALS +/- .010
3 PL DECIMALS +/- .005
THIRD ANGLE PROJECTIONS

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SIGNATURES		DATE
DRAWN	PRAO	02/26/16
CHECKED	AKAP	02/26/16
ENGRG	AKAP	02/26/16
ISSUED		

CYPRESS SEMICONDUCTOR
198 CHAMPION COURT
SAN JOSE, CA 95134
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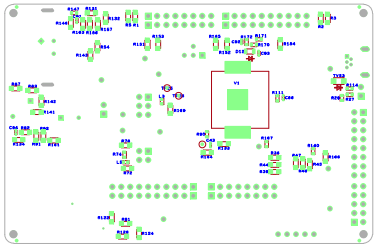
ASSEMBLY TOP LAYER
CY8CKIT-048 PSoC ANALOG COPROCESSOR KIT

SIZE: C | FSCM NO: | DWG NO: 620-60302-01 | REV: 06

SCALE: | SHEET:



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ASSEMBLY BOTTOM LAYER CY8CKIT-048 PSoC ANALOG COPROCESSOR KIT

SIZE	FSCM NO	DWG NO	REV
C		620-60302-01	06

SCALE: | SHEET: 2 OF 2